SDS

Scientific Data Systems
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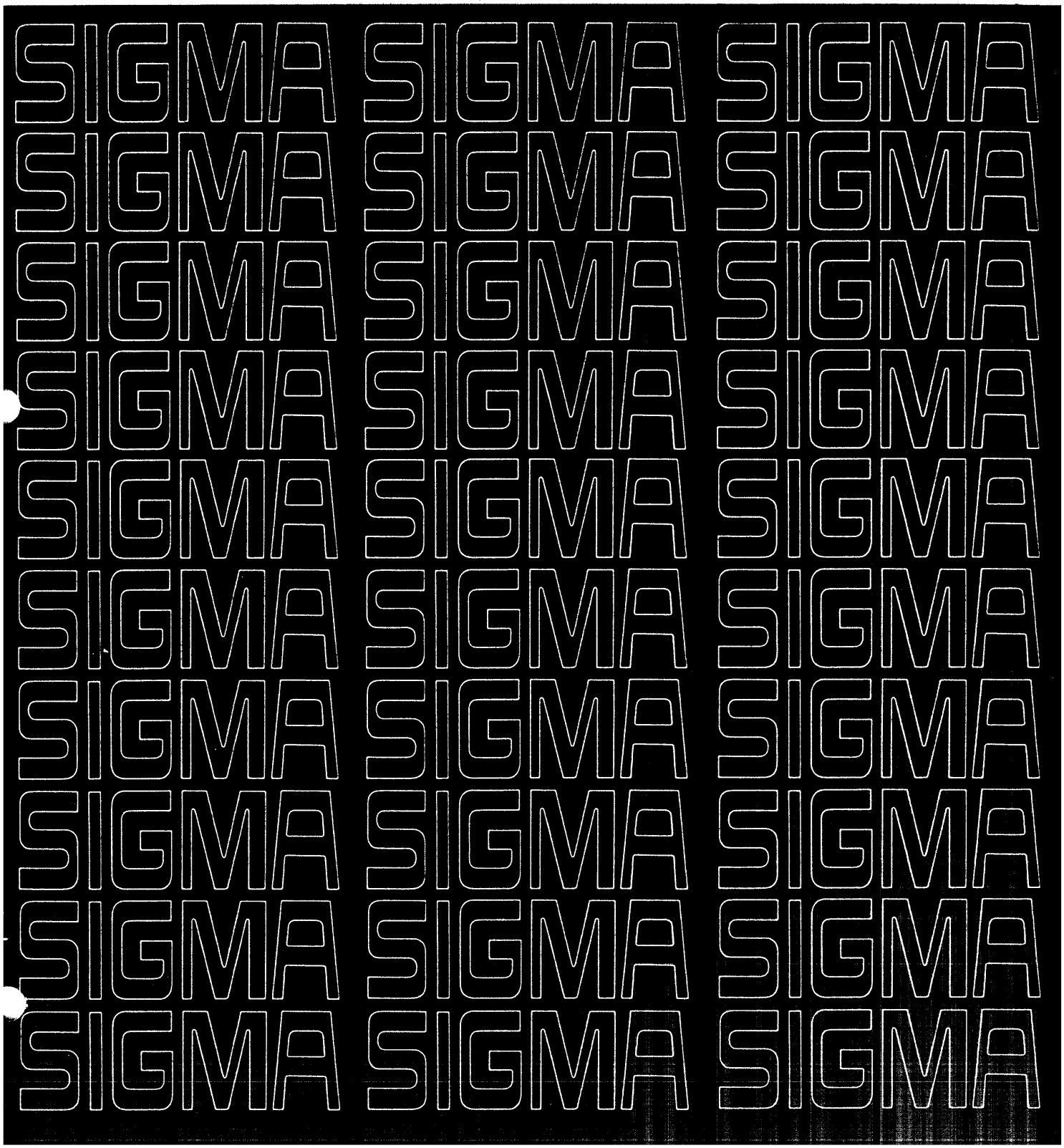
XDS SIGMA RAD STORAGE SYSTEM
MODELS 7201/7202/7203/7204

Reference Manual



RAD ORDER CODES

Code (Hexadecimal)	Function
01	Write
02	Read (Report any transmission error at "count done")
03	Seek
04	Sense
05	Check-write
12	Read (Terminate data transfer and report any transmission error at end of current sector if error is encountered)

Price: $ .75

RAD STORAGE SYSTEM

MODELS 7201/7202/7203/7204

REFERENCE MANUAL

for

XDS SIGMA COMPUTERS

90 09 79C

October 1969

XDS

Xerox Data Systems/701 South Aviation Boulevard/El Segundo, California 90245

Printed in U.S.A.

REVISION

This publication, 90 09 79C, is a revision of the XDS Sigma RAD Storage System Reference Manual, 90 09 79B. Changes to the previous manual are indicated by a vertical line in the margin of the affected page.

RELATED PUBLICATIONS

Title	Publication No.
XDS Sigma 2 Computer Reference Manual	90 09 64
XDS Sigma 3 Computer Reference Manual	90 15 92
XDS Sigma 5 Computer Reference Manual	90 09 59
XDS Sigma 7 Computer Reference Manual	90 09 50
XDS Sigma 5/7 Symbol and Meta-Symbol Reference Manual	90 09 52
XDS Sigma 2 Symbol Reference Manual	90 10 51

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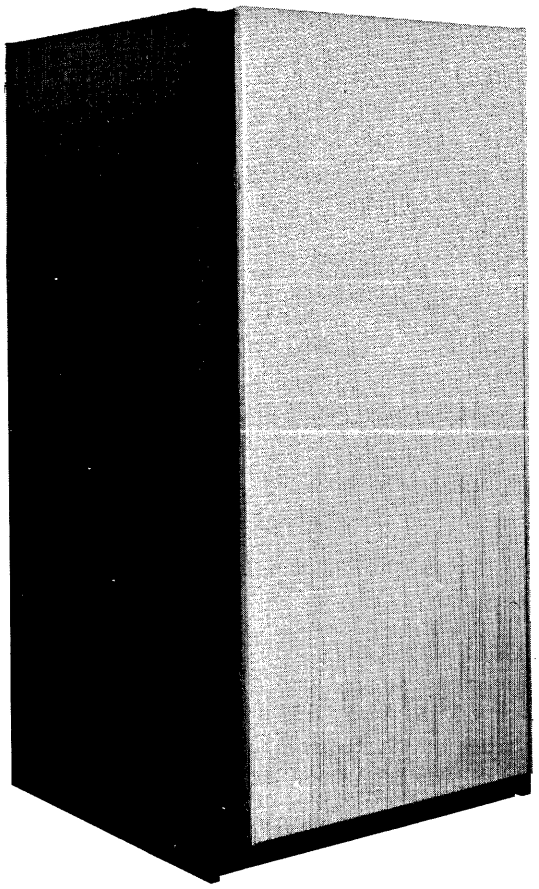
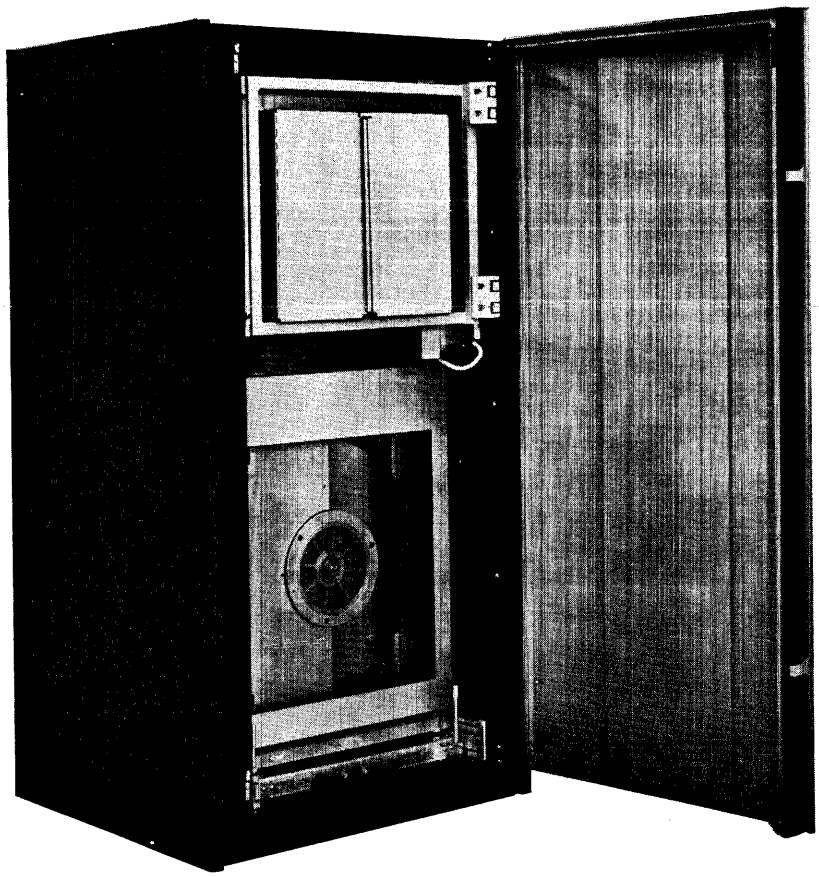


Model 7201 RAD Controller and 7204 Storage Unit



RAD Interior View

1. GENERAL DESCRIPTION

INTRODUCTION

The RAD (Rapid Access Data) Storage System provides fast, auxiliary, random-access memory for XDS Sigma computers. RAD units may be used for system, scratch pad, or working storage for processing programs. In a time-sharing system, they may serve as permanent file storage, "swap" storage, and as a medium for storing real-time programs.

A RAD system consists of one Model 7201 Controller and one to eight storage units, either Model 7202, 7203, or 7204. The controller and one storage unit are in the same cabinet. Additional storage units are in separate cabinets.

The basic addressable unit of information is a sector of 360 data bytes. There are 16 sectors to each track. A RAD unit may have 128, 256, or 512 tracks depending on the model. Data is presented in 8-bit bytes to the RAD by the controlling system, and each byte is written serially on the selected sector. Access time is minimal because each track has a separate read/write head (average access time is 17 milliseconds).

Rotational delay may be reduced by sensing the unit's current position before initiating an input or output operation and then transferring data beginning immediately at the next sector to be accessed. If desired, a data record can overlap from sector to sector or from track to track; the RAD controller automatically performs sector and track incrementing.

The contents of RAD storage units are permanently protected against primary power failure. Also, "write-protect" switches prevent inadvertent destruction of recorded information due to programming error. Each switch inhibits writing on 32 adjacent tracks.

The term "RAD" in this manual indicates a device controller and storage unit. Any separate reference is specified by "controller" or "storage unit".

To use this manual effectively, the reader should be familiar with the Sigma Computer Reference Manual (see Related Publications, page ii) applicable to his installation (particularly the input/output instructions and input/output operations sections).

TYPICAL CHARACTERISTICS

RAD file rotational speed	1774 rpm
Total time per revolution	33.8 milliseconds
Inter-sector gap time	180 microseconds
Sector-to-sector time	2.11 milliseconds
Effective read/write bit rate	1,500,000 bits/second
Byte transfer rate	187,500 bytes/second (maximum) 170,500 bytes/second (average)
Byte capacity	
Model 7202	737,280 bytes (128 tracks)
Model 7203	1,474,560 bytes (256 tracks)
Model 7204	2,949,120 bytes (512 tracks)
Write protection	Each switch protects 32 tracks (for all models)
Cabinet dimensions	Height – 63 in. Width – 30 in. Depth – 29 in.
Power requirements	Service – 208 vac ± 10%, three-phase, 60 ± 0.5 Hz Start – 20 kva Run – Controller, 250 watts Storage Unit, 1100 watts
Ambient temperature	50° to 105° F.
Relative humidity	10% to 90%

2. FUNCTIONAL DESCRIPTION

DATA REPRESENTATION

Data is presented to a RAD one byte at a time, and is written bit-serially on the designated sector. Similarly, data is read serially from a RAD and assembled in its buffer register for presentation to the controlling system, a byte at a time. (See "RAD Orders" and "Addressing Format".)

RAD STATES

The RAD's initial operational state depends on its power status. If all power is off, it is removed from the line ("not operational" state). Any attempt to access it results in a response of "No I/O address recognition" to the I/O instruction. The status response, if requested, is unpredictable under these conditions.

OPERATIONAL STATES

When required power is on, the RAD enters the "automatic" mode and the "ready" condition. The exact RAD condition may be determined by examining the status response to one of the instructions, START INPUT/OUTPUT (SIO), HALT INPUT/OUTPUT (HIO), or TEST INPUT/OUTPUT (TIO). Other I/O instructions, TEST DEVICE (TDV) and ACKNOWLEDGE INPUT/OUTPUT INTERRUPT (AIO), provide additional specific status indications (see "RAD Status Response"). A brief explanation of RAD conditions and modes follows.

CONDITIONS

Ready. The "ready" condition is entered when required power is initially turned on. In this condition, an SIO instruction can be accepted by the RAD controller and executed, provided that no interrupt is pending.

Busy. In this condition, the RAD controller has already accepted an SIO instruction. A new SIO will not be accepted until the current operation is completed and no device interrupt is pending.

MODES

Automatic. The RAD is in the "automatic" mode as long as required power is on ("ready-automatic" or "busy-automatic").

TRANSITIONS BETWEEN STATES

Table 1 summarizes the allowable state transitions and the conditions required to cause them.

Table 1. RAD Controller State Transitions

Present State \ Next State	Not Operational	Ready Automatic	Busy Automatic
Not Operational	———	Power is turned on	Not possible
Ready Automatic	Power is turned off	———	SIO has been accepted
Busy Automatic	Power is turned off	Operation completed, or HIO, or I/O reset signal received	———

DATA TRANSFER

A RAD operation is initiated by the controlling system with a START INPUT/OUTPUT OPERATION (SIO) instruction if all the following conditions are satisfied:

1. Input/output address recognition exists.
2. The RAD is in the "ready" condition.
3. No RAD interrupt is pending.

If these are satisfied, the RAD enters the "busy" condition. The RAD controller now initiates the transfer of data to or from the RAD storage unit as specified by the order (Write or Read) until the required number of bytes have been transferred. The operation then terminates, and the RAD returns to the "ready-automatic" state. The operation may also be terminated:

1. By an Input/Output Processor (IOP) Halt[t], generated by the IOP[t] on certain error conditions (in which case all data may not have been transferred).
2. By a HALT I/O (HIO) instruction (in which case all data may not have been transferred).

Following an HIO or IOP Halt[t], the RAD is in a "ready-automatic" state.

[t] Not applicable to Sigma 2.

3. PROGRAM INTERFACE

RAD ORDERS

The RAD contains an address register that selects the track and sector to be accessed. This register is initially loaded by executing a Seek order. During a data transfer, if more bytes are transferred than can be contained in one sector (360 bytes) the address register is automatically incremented so that the next sector is addressed. An error results, however, if the address register is incremented when addressing the last available sector. This error condition also occurs if a programmer tries to use a Seek order to load the address register with a nonexistent sector.

Upon completion of a data transfer, the address register is incremented so that it addresses the sector following the last one accessed.

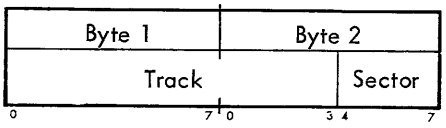
During a write operation, each byte received is summed to form a parity check byte. This byte is always written in the last byte position of the sector, even if less than 360 bytes are transmitted. During a read operation, the data is summed as it is read and the resulting sum is compared with the parity check byte. Failure to compare results in an error condition.

The six valid orders are:

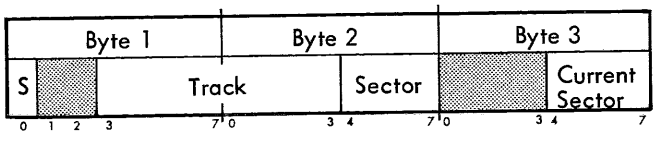
Order	Action
X'01' Write	The Write order causes the RAD unit to record the number of bytes specified in the command doubleword, starting at the track and sector address currently selected by the RAD controller address register (this address is specified by the previous Seek order or the last sector accessed incremented by one). Transmission continues until the computer indicates to the storage unit that the entire record has been transferred. If the transmitted information does not completely fill the last sector, zeros are written into the remainder of the sector. If a write operation is attempted in a protected area, the operation is not performed and the condition is immediately reported to the controlling system (see "Addressing Format" and "RAD Status Response" in this section).
X'02' Read	This Read order causes the RAD to read the bytes specified in the command doubleword, starting at the track and sector address currently selected by the RAD controller address register (this address is specified by the previous Seek order or the last sector accessed incremented by one). The data is stored in core memory at the location specified by the command doubleword. Any transmission errors are signalled at the end of the logical record.
X'12' Read	This Read order reads the number of bytes specified in the command doubleword from the track and sector currently selected by the RAD controller address register (this address is specified by the previous Seek order or the last sector accessed incremented by one). The data is stored in core memory starting at the location specified by the command doubleword. Any transmission errors are signalled at the end of the current sector.
X'03' Seek	The Seek order causes two bytes to be sent to the RAD where they are loaded into the RAD controller address register. The controller then directs any subsequent read/write operation to begin at this address. An "incorrect length" indication is generated if a byte count other than 2 is specified in the I/O doubleword associated with the Seek order.
X'04' Sense	The Sense order causes the storage unit to transmit three bytes of position and status information into core memory. The first two bytes are the contents of the RAD address register currently stored in the controller. The first bit of the first byte indicates whether the track associated with the current track address is "write-protected". The third byte indicates the current rotational position of the last unit addressed. Incorrect length indication is generated if a byte count other than 3 is specified in the I/O doubleword associated with the Sense order.
X'05' Check-write	The Check-write order is used to verify recorded data. It causes data to be sent to the RAD controller by the controlling system where it is compared with that being read from the RAD. In the event that a byte does not compare, a "transmission error" signal is transmitted to the controlling system, and the data transfer is terminated. Data on the RAD and in core storage are not recorded or modified, but only compared.

ADDRESSING FORMAT

The format of the two bytes sent to the RAD by a Seek order is:



The format of the three bytes received on a Sense order is:



where

S is the setting of the write-protect switch for the indicated track (0 = not write-protected; 1 = write-protected).

Track is the track number selected by the RAD controller address register.

Sector is the sector number selected by the RAD controller address register.

Current sector is the current sector position of the RAD.

KEY EVENTS

The key events that occur during a RAD operation are described in the following paragraphs. No chronological order of occurrence should be assumed from the order of presentation.

START INPUT/OUTPUT

A RAD operation is initiated with the execution of an SIO instruction by the controlling system. If I/O address recognition exists and the RAD is in the "ready" condition with no interrupt pending, the controlling system sets its "I/O address recognition" and "SIO accepted" indicators. The RAD then advances from the "ready" to the "busy" condition. It then requests an order byte from the controlling system and proceeds with the operation defined by the order byte.

UNUSUAL END CONDITIONS

Detecting any of the following conditions after receiving an order causes the RAD to return an "unusual end" indication to the controlling system when the condition occurs:

1. Invalid order code
2. Power failure in the addressed unit
3. Incrementing the RAD controller address register beyond the last available sector in the current RAD unit
4. Nonexistent "Seek" address
5. Attempting to write on a write-protected track
6. Transmission data error

CHANNEL END CONDITIONS

After receiving an order from the controlling system, the RAD signals "channel end" to the controlling system when all data has been transferred or when an "unusual end" condition occurs while a data transfer is in process.

FAULT CONDITIONS

A fault condition is any condition that causes a peripheral device to become "not operational". Absence or failure of ac or dc power causes the RAD to become "not operational".

TRANSMISSION ERROR CONDITIONS

The RAD can detect and report transmission errors to the controlling system. Conditions causing this error are:

1. Failure of the end of sector parity check during a read operation.
2. Failure of a data comparison on a Check-write operation (the parity byte is also automatically compared).
3. A data overrun; the controlling system has failed to maintain the data transfer rate required by the RAD during the execution of the previous Read, Write, or Check-write order.
4. Failure to recognize a "sync" pattern on a Read or Check-write order.

INCORRECT LENGTH CONDITIONS

The RAD can detect and report incorrect length errors to the controlling system. Conditions causing this error are:

1. A byte count other than 2 has been specified in the I/O doubleword associated with a Seek order.
2. A byte count other than 3 has been specified in the I/O doubleword associated with a Sense order.
3. The last Read, Write, or Check-write order did not specify a byte count that was an integral multiple of 360 bytes.

RAD STATUS RESPONSE

The RAD system returns various status flags in response to computer-executed I/O instructions. A detailed explanation of the I/O instructions and their status information is contained in the reference manuals for Sigma computers. The following paragraphs explain the significance of each status flag returned to the controlling system.

I/O INSTRUCTION STATUS BITS

The execution of an I/O instruction by the controlling system provides two bits of immediate information pertaining to the general status of the addressed I/O device and its controller. This information is retained by the controlling system in a form that allows for conditional branching based on the response of the device (and its controller) to the I/O instruction. Table 2 lists the possible status bit settings provided by the execution of each I/O instruction and the significance of each setting.

Table 2. RAD I/O Instruction Status Bits

Instruction	Status Bits[t] CC1 or O	CC2 or C	Significance
SIO	0	0	I/O address recognized and SIO accepted (i.e., RAD has entered the "busy" condition).
	0	1	I/O address recognized but SIO not accepted (i.e., RAD was already "busy" or a device interrupt is pending).
	1	0	RAD is attached to a "busy" selector IOP.[tt]
	1	1	I/O address not recognized.
HIO	0	0	I/O address recognized and the RAD was not "busy" when the halt occurred.
	0	1	I/O address recognized and the RAD was "busy" when the halt occurred.
	1	1	I/O address not recognized.
TIO	0	0	I/O address recognized and SIO can currently be accepted (i.e., RAD is in the "ready" condition with no device interrupt pending).
	0	1	I/O address recognized but SIO can not currently be accepted.
	1	0	RAD is attached to a "busy" selector IOP.[tt]
	1	1	I/O address not recognized.
TDV	0	0	I/O address recognized and previous operation was not terminated because of a fault condition.
	0	1	I/O address recognized but previous operation was terminated because of a fault condition.
	1	0	RAD is attached to a "busy" selector IOP.[tt]
	1	1	I/O address not recognized.
AIO	0	0	Normal interrupt (i.e., "channel end" or "zero byte count") condition present.
	0	1	Unusual interrupt (i.e., "fault") condition present.
	1	1	No interrupt condition present

[t]The symbols "CC1" and "CC2" refer to condition code bits in Sigma 5/7 computers. The symbols "O" and "C" refer, respectively, to overflow and carry indicators in Sigma 2/3 computers.

[tt]This condition is not applicable to Sigma 2/3 computers.

DEVICE STATUS BYTE

The following eight bits of information are made available to the controlling system in response to the execution of an I/O instruction.

STATUS RESPONSE FOR SIO, TIO, AND HIO

Bit 0: Device Interrupt Pending. If this bit is a 1, an interrupt call is pending (issued but not yet acknowledged by an AIO instruction). The RAD continues to transmit data (if specified) until the current operation is completed (all data transferred or operation terminated due to an error condition), but does not accept a new SIO instruction until this interrupt has been acknowledged. However, a new order can be accepted, if command chaining is specified, even though an interrupt may be pending. The interrupt may be cleared by executing an AIO or HIO instruction.

Bits 1-2: RAD Storage Unit Condition. The RAD storage unit condition is indicated by these bits:

Flags	Condition
00	RAD Ready – The RAD storage unit is inactive; i.e., it is not engaged in a data transfer operation.
01	RAD Not Operational – Power is not applied to the RAD storage unit or it is off-line for testing purposes.

Flags	Condition
10	Device Unavailable – This condition is not applicable to the RAD.
11	RAD Busy – The RAD storage unit is currently active, i.e., it is engaged in a data transfer operation through the controller.

Bit 3: Mode-Automatic or Manual. This bit is always a 1, indicating "automatic" mode.

Bit 4: Device Unusual End. This bit is a 1 if the previous operation terminated due to an abnormal condition, as listed under "Unusual End Conditions".

Bits 5-6: RAD Controller Condition. The RAD controller condition is indicated by these bits:

Flags	Condition
00	RAD Controller Ready – The RAD Controller is capable of accepting an SIO instruction, if no interrupt is pending (and no storage unit is busy).
01	Device Controller Not Operational – This condition is not applicable to the RAD.
10	Device Controller Unavailable – This condition is not applicable to the RAD.
11	RAD Controller Busy – The RAD controller is currently executing a previous order (one storage unit is also busy).

Bit 7: Unassigned. This bit is currently unassigned and is always reset to 0.

STATUS RESPONSE FOR TDV AND AIO

Bit 0: Data Overrun. If this bit is a 1, a data overrun has occurred during execution of the previous order (see "Transmission Error Conditions").

Bit 1: Unassigned. This bit is currently unassigned and is always reset to 0.

Bit 2: Sector Unavailable. If this bit is a 1, the RAD controller address register was incremented beyond the last available sector during the previous order, or a Seek order loaded the RAD controller address register with a value greater than the last available sector.

Bit 3: Write-protect Violation. If this bit is a 1, the previous Write order attempted to write on a track that was write-protected.

Bit 4: Missed "Sync" Pattern. This bit is for diagnostic use only.

Bits 5-7: Unassigned. These bits are currently unassigned and are always reset to zeros.

OPERATIONAL STATUS BYTE

In addition to the information contained in the Device Status Byte, the following indicators are made available to the controlling system at the conclusion of each operation (see the applicable Sigma Computer Reference Manual for detailed information).

INCORRECT LENGTH

If this flag is a 1, an incorrect length condition has occurred since the previous order was received by the RAD.

TRANSMISSION DATA ERROR

If this flag is a 1, one of the conditions specified under "Transmission Error Conditions" has occurred since the previous order was received by the RAD.

CHANNEL END

If this flag is a 1, the RAD has terminated its operation for any of the reasons listed under "Channel End Conditions".

UNUSUAL END

If this flag is a 1, the RAD has terminated its operation for any of the reasons listed under "Unusual End Conditions".

PROGRAMMING CONSIDERATIONS

This RAD system is designed to permit track switching and order modification (read to write and vice versa) during the gap between sectors. The command chaining feature of the I/O system must be used.†

Frequent data chaining (small byte counts) or frequent use of test instruction loops (TIO's and TDV's) causes a reduction of the available I/O system transfer rate due to the additional communication between the I/O section and the central processor and/or memory required for either kind of task. This can result in a reduction of as much as 50 percent and, therefore, can cause frequent data overruns.

When "immediate" mode transfer techniques are used (data transmission at the next available sector) the programmer must add 1 to the sector number received as a result of the Sense order. This procedure ensures one sector time (2.11 milliseconds) for the programmer to prepare the command list for the subsequent data transfer. Command chaining should be used between the ensuing Seek order and the related data operation, i.e., Read, Write, or Check-write. If command chaining is not used, 2 must be added to the sector number received from the Sense order, or the time of

†Command chaining not available on the Sigma 2/3 I/O system.

one revolution of the RAD will be lost before data transfer is initiated.

INFORMATION PROTECTION

The contents of RAD storage units are protected in case of primary power failure; recorded information is not lost or altered.

"Write-protect" switches prevent inadvertent destruction of recorded data due to programming error. These toggle switches are located on a panel inside the cabinet. Writing is inhibited with the switch in the "up" position. Each switch protects 32 tracks. The first switch inhibits writing on tracks 0 through 31; the second inhibits writing on tracks 32 through 63, etc.

SEQUENCE OF ACTIVITY

The following figures illustrate the sequential relationship of the key events that occur during RAD operations.

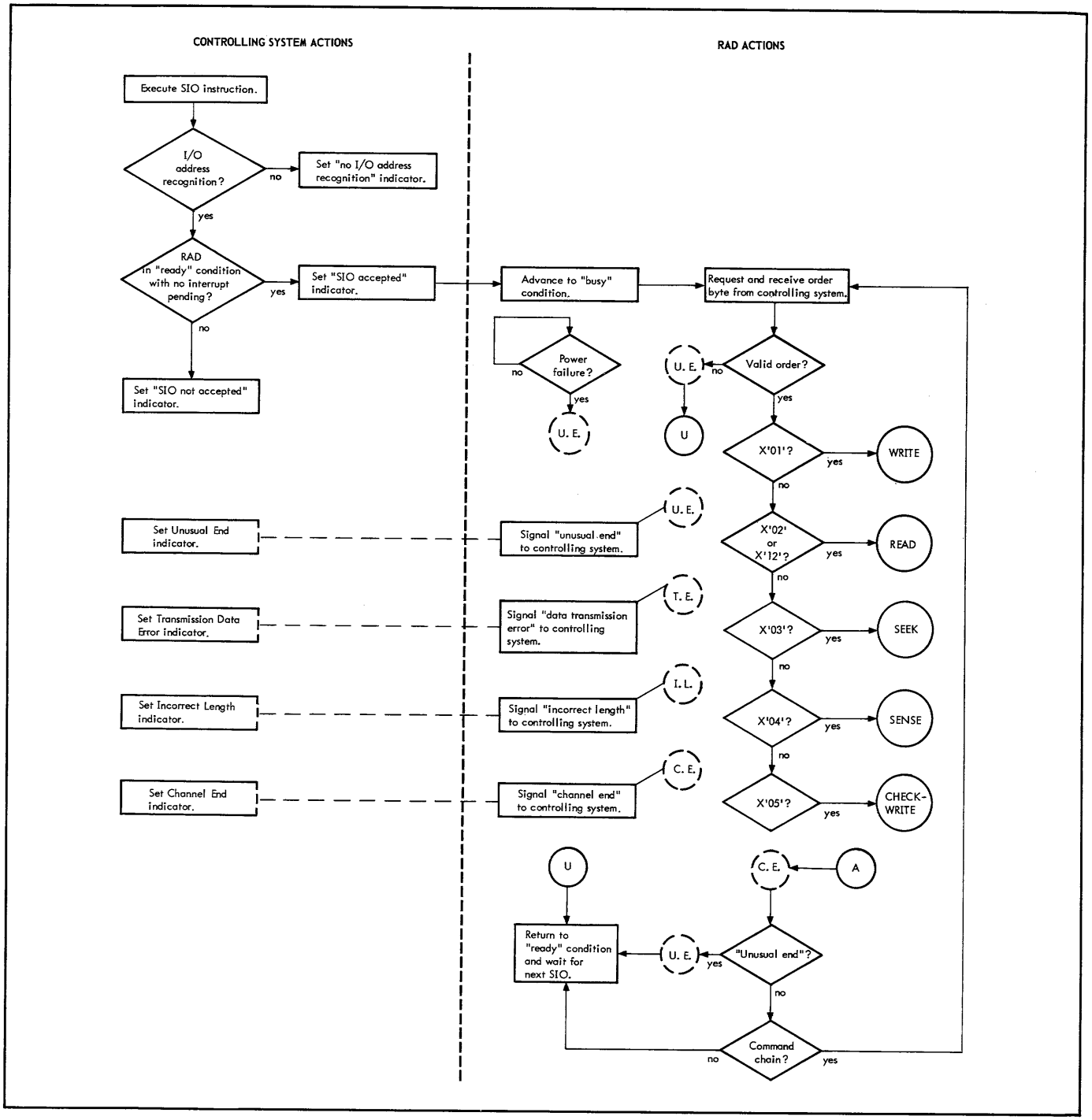


Figure 1. Controlling System/RAD Actions

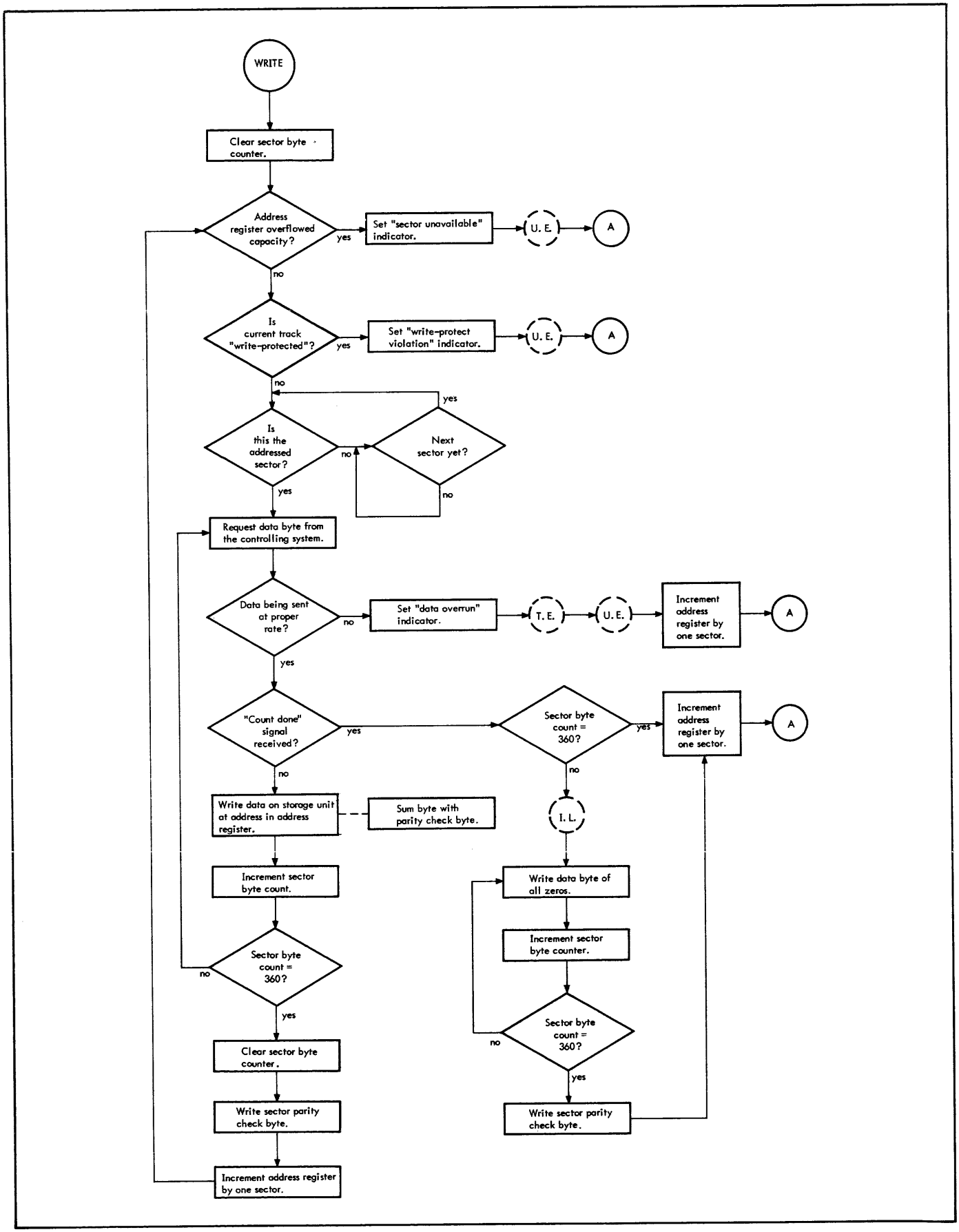


Figure 2. Write Order RAD Actions

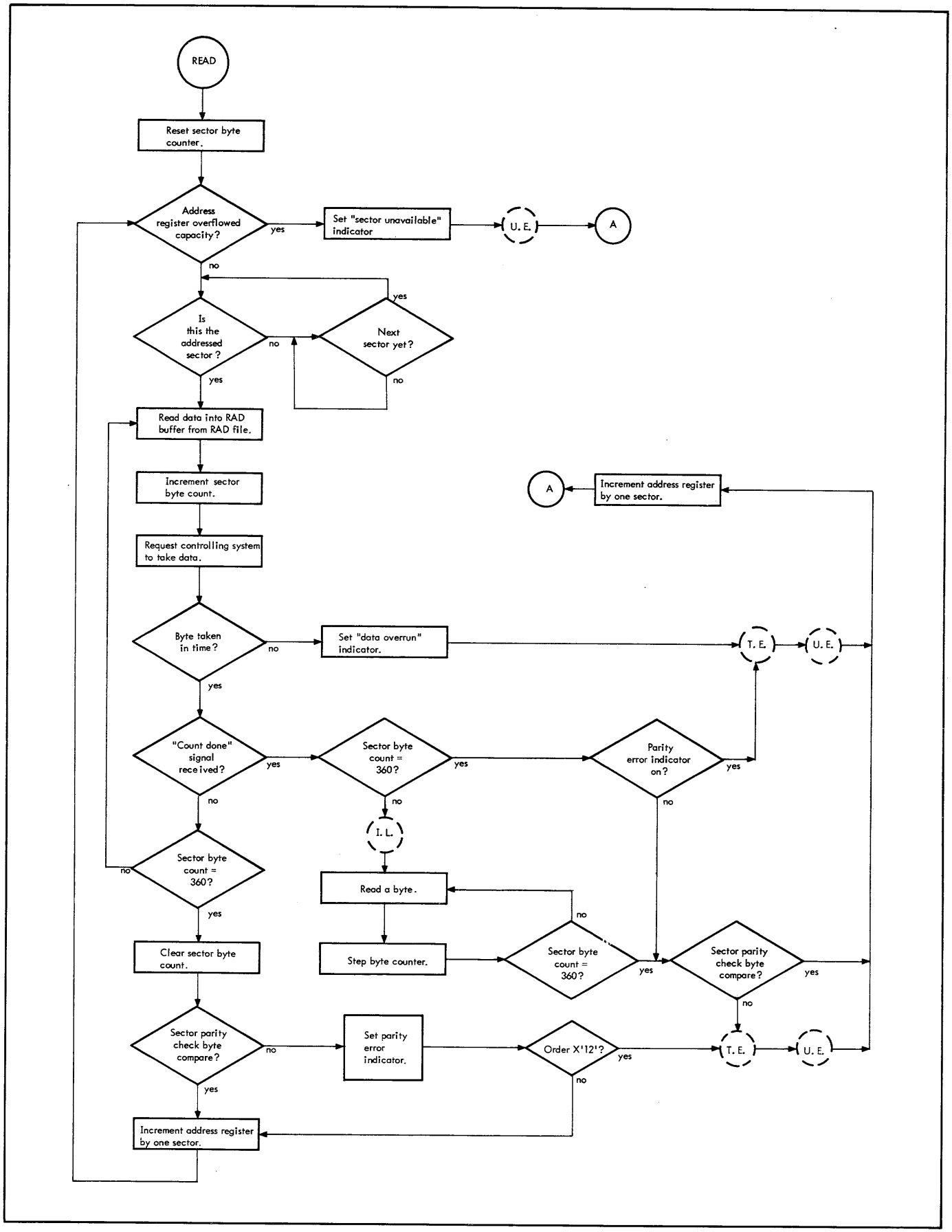


Figure 3. Read Order RAD Actions

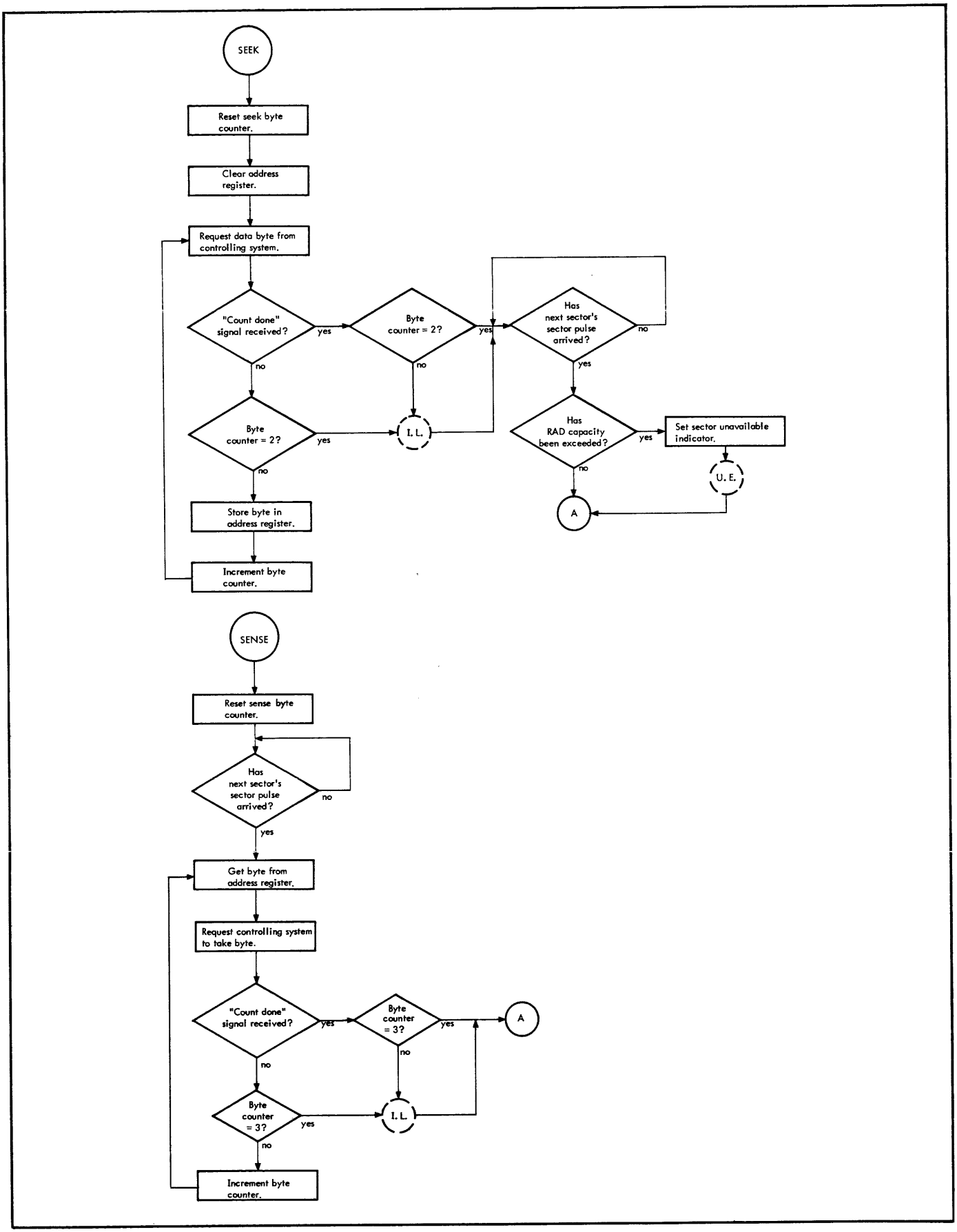


Figure 4. Seek/Sense Order RAD Actions

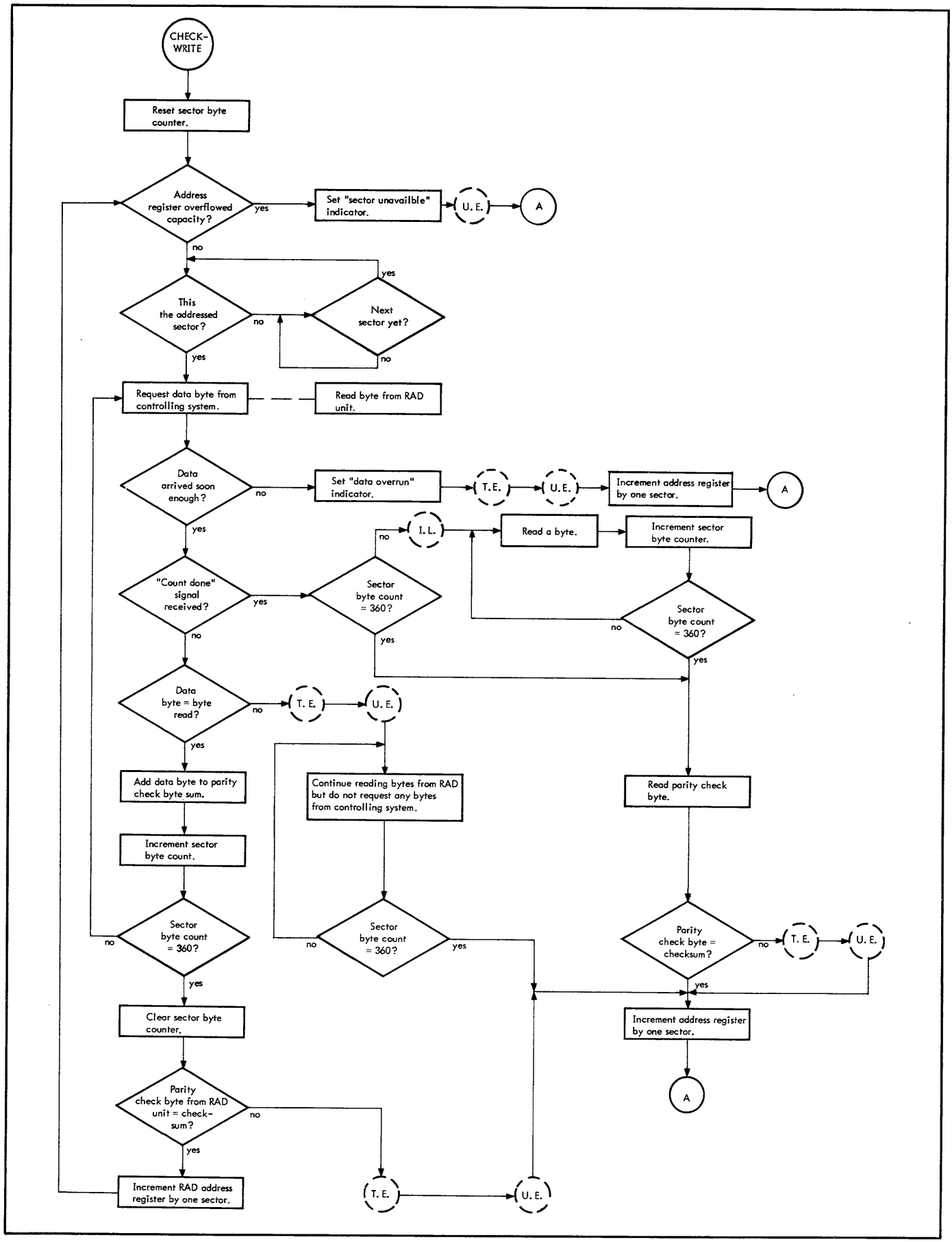


Figure 5. Check-write Order RAD Actions

APPENDIX

SIGMA 5/7 PROGRAMMING EXAMPLE

The following example is a subroutine for reading or writing data on the RAD in a Sigma 5 or 7 computer system. The subroutine assumes that the RAD is the only I/O device currently being used and that the main program sets up locations indicating the storage unit address, track and sector address, address of the I/O area in main core memory, and the number of bytes to be transferred.

The subroutine is called with the instruction BAL,15 RADREAD or BAL,15 RADWRITE. There are three possible returns that the subroutine can make to the main program:

1. If the operation is completed normally, return to calling location + 1.
2. If the operation cannot be started ("no I/O address recognition" or "SIO not accepted") return to calling location + 2.
3. If an error occurs during or upon completion of the operation, return to calling location + 3.

Label	Command	Argument	Comments
RADREAD	LD,R8	RDSORDER	Load R8 and R9 with read command pair.
	LI,R10	-1	Set read-write indicator for read.
	B	$ + 3	
RADWRITE	LD,R8	WRTORDER	Load R8 and R9 with write command pair.
	LI,R10	0	Set read-write indicator for write.
	OR,R8	BFRADDRS	Set up memory byte address (the main program stores an address in "BFRADDRS" before branching here).
	OR,R9	BYTCOUNT	Set up byte count (the main program sets this location before branching here).
	STD,R8	COMMLIST + 2	Save assembled command pair in command list.
	MTW,0	R10	
	BCS,1	IOINTSUP	Is this a write operation?
	LD,R8	COMMLIST + 6	Yes – set up check-write command pair.
	AND,R8	FLAGMASK	Save order field.
	AND,R9	FLAGMASK	Save flag field.
	OR,R8	BFRADDRS	Set up memory byte address.
	OR,R9	BYTCOUNT	Set up byte count.
	STD,R8	COMMLIST + 6	Store check-write command pair in command list.
IOINTSUP	LW,R8 STW,R8	DSCIOINT X'5C'	Get and store an "XPSD DSCINTPT" instruction into location 5C.
	LI,R8	X'20'	Set I/O interrupt arming bit.
	WD,R8	X'1200'	Arm and enable the I/O interrupt.
	LI,R0	DA(COMMLIST)	Load register 0 with the doubleword address of the first command pair in the command list.
	SIO,R10	*DISCADDR	Start disc operation ("DISCADDR" is set up by the main program and is the disc "unit address").
	STCF	DSCCSAVE	Save the condition code for the SIO.
	BCR,12	$ + 3	Was SIO accepted?
	MTW,1 B	R15 *R15	No – step return address once and return to the main program.

Label	Command	Argument	Comments
	WAIT		Yes – wait for the I/O interrupt.
DISCDONE	AIO,R10	0	Acknowledge the interrupt.
	STCF	DSCCSAVE	Save the AIO condition code
	LCF	DSCCSAVE	Get saved condition code.
	BCR,4	$ + 2	Did operation finish successfully?
	MTW,2	R15	No – add 2 to return address.
DISCEXIT	LI,R8	X'20'	Yes – disable and disarm the I/O interrupt.
	WD,R8	X'1100'	
	B	*R15	Return to the main program.
	:		
	BOUND	8	This is an assembler directive insuring that the following constants are on a doubleword boundary
RDSORDER	DATA	X'02000000'	Read command pair-flags = interrupt on channel end or
	DATA	X'1E000000'	unusual end, halt on transmission error, and suppress incorrect length.
WRTORDER	DATA	X'01000000'	Write command pair-flags = command chain, interrupt
	DATA	X'2E000000'	on unusual end, halt on error, and suppress incorrect length.
COMMLIST	DATA	X'03000800'	Seek command pair – the address 800 is the byte address
+1	DATA	X'2E000002'	of a location (200) where the main program stores the track and sector address for the read or write operation, the byte count is 2, and the flags are the same as the write flags above.
+2	DATA	0	The read or write command pair are stored here.
+3	DATA	0	
+4	DATA	X'03000800'	Seek command pair – this command is used on a write
+5	DATA	X'2E000002'	operation and is identical to the one above.
+6	DATA	X'05000000'	Checkwrite command pair – this command pair is exe-
+7	DATA	X'1E000000'	cuted on a write operation to verify data on the disc from the write just executed.
FLAGMASK	DATA	X'FF000000'	"Order" and "flag" field mask.
DSCIOINT	XPSD	DSCINTPT	This instruction is stored in X'5C'.
DSCINTPT	DATA	0	When the I/O interrupt occurs, the program status double-
	DATA	0	word is saved in "DSCINTPT" and "DSCINTPT + 1" and
	DATA	DISCDONE	the program branches to "DISCDONE".
	DATA	0	
DSCCSAVE	DATA	0	Temporary storage for condition code.
	:		
	MAIN PROGRAM		
BFRADDRS	DATA	---	This location contains the address of the I/O buffer area.
BYTCOUNT	DATA	---	This location contains the byte count.
DISCADDR	DATA	---	This location will contain the unit address.
	:		

Label	Command	Argument	Comments
	BAL,15	RADREAD	Call (branch to) RAD read routine; save return address in general register 15.
	B	RDONE or $ + 3	Normal return.
	B	RABNORM	Abnormal return (no I/O address recognition or RAD not operational).
	B	RERROR	Error return.
	:		
	:		
	BAL,15	RADWRITE	Call RAD write routine; save return address in general register 15.
	B	WDONE	Normal return.
	B	WABNORM	Abnormal return.
	B	WERROR	Error return.

SIGMA 2/3 PROGRAMMING EXAMPLE

The following example is a subroutine showing one way in which the RAD in a Sigma 2 or 3 computer system could be programmed. It assumes that no other I/O devices are in operation and certain locations have been set up by the main program before the subroutine is called. The subroutine is called with the instruction sequence:

```
RCPYI 1,2                    RCPYI 1,2
B     RADWRITE     or        B     RADREAD
```

There are three possible returns to the main program:

1. If the operation is completed normally, return to calling location + 1 in the main program.
2. If the operation cannot be started, return to calling location + 2.
3. If an error is encountered during or after the operation, return to calling location + 3.

The maximum record length that can be written or read in this routine is 8191 bytes. The data will be stored in a block of core memory, labeled "IOBUFFER", during a read operation. For a write operation, the data should be in this same area of main core memory prior to branching to this routine.

Label	Command	Argument	Comments
RADWRITE	LDA	WRITE	Get Write order.
	B	$ + 2	
RADREAD	LDA	READ	Get Read order.
	STA	ORDER	Save specified order.
	RCPY	2,7	Save the return address to the main program in location "RADRETN".
	STA	RADRETN	
	LDA	RADADDRS	Execute a TIO instruction to the unit addressed in location
	TIO		"RADADDRS" which is the unit address of the RAD.
	STA	TIOSTAT	Save TIO status response.
	RD	X'C0'	Save overflow and carry bits.
	AND	= 3	
	STA	TIOSTAT + 1	Save O and C indicators.
	BAZ	$ + 2	Overflow or carry set?
	B	EXIT - 1	Yes – Return to branch address + 2.
	LDA	RADADDRS	No – Generate the addresses of the even and odd channel registers
	SCRS	3	for the unit addressed by "RADADDRS" (I/O channel x 2 + 8 = E;
	AND	=X'E'	I/O channel x 2 + 9 = O). Save these addresses in locations
	ADD	=8	"ECHANNEL" and "OCHANNEL", respectively.
	STA	ECHANNEL	
	RCPYI	7,7	
	STA	OCHANNEL	
	LDA	=SEEK	Set the word address of the Seek I/O table in the even channel
	WD	*ECHANNEL	register.
	LDA	=3	Set the byte count for the Seek operation in the odd channel reg-
	WD	*OCHANNEL	ister (Order byte + 2 data bytes.)
	LDA	RADADDRS	Load accumulator with device address.
	SIO		Issue SIO to the addressed device.
	TIO		
	BNO	$ + 2	New SIO possible?
	B	$ - 2	No – Execute TIO again.

Label	Command	Argument	Comments
	RD	*ECHANNEL	Yes – Get operational status byte.
	AND	=X'C800'	Save TE, IL, and UE bits.
	RCPY	7,6	Save these bits in the extended accumulator.
	LDA TDV ROR	RADADDRS 6,7	Get the device status and combine with the opearional status byte indicators.
	BAZ	$ + 2	Did an error occur during the Seek?
	B	EXIT - 2	Yes – Return to branch address + 3.
	LDA STA	=RADINTPT X'106'	No – Store the interrupt processor starting address in the I/O interrupt location.
	LDA	=X'200'	Set I/O interrupt bit in accumulator.
	WD	*INTCNTL	Arm and enable the I/O interrupt.
	LDA WD	=ORDER *ECHANNEL	Set even I/O channel to the address of the specified order.
	LDA WD	=X'6001' *OCHANNEL	Set odd I/O channel for 1 byte (order) and set the data chaining and interrupt bits.
	LDA OR	COUNT =X'2000'	Set interrupt flag in odd channel word with byte count.
	STA	ORDER + 2	Save odd channel word.
	LDA	RADADDRS	Execute the specified order.
	SIO		
WAIT	WAIT		Wait for interrupt at channel end time.
RADINTPT	DATA DATA	0 0	These two locations are to hold the Program Status Doubleword at the time the interrupt occurs.
	LDA WD	=X'200' *INTCNTL1	Disarm the I/O interrupt.
	AIO STA RD AND STA	 AIOSTAT X'C0' =3 AIOSTAT+1	Execute an AIO and save the status and address response. Save the overflow and carry indicators.
	LDA	RADADDRS	Get device address.
	TIO		Get I/O status.
	AND	=X'6000'	Save device status bits.
	CP	=X'6000'	Check for "busy".
	BNC	$ + 5	Is device "busy"?
	LDA WD	=X'200' *INTCNTL	Yes – arm and enable the I/O interrupt.
	WD LDX	X'D8' INTCNTL1	Go back to WAIT until a "channel end" occurs.
	RD	*ECHANNEL	Get Operational Status Byte.
	AND STA	=X'C800' ERRSAVE	Save TE, IL, and UE bits.
	OR	AIOSTAT	Add AIO error bits.
	BAZ	$+3	Did an error occur on this operation?

```
Label       Command     Argument      Comments
            WD          X'D8'         Yes – Clear interrupt and return to branch address + 3.
            LDX         ERREXIT
            WD          X'D8'         No – Clear interrupt and return to branch address + 1.
            LDX         NOERXIT
            IM          RADRETN       Return to calling location + 3.
            IM          RADRETN       Return to calling location + 2.
EXIT        B           *RADRETN      Return to calling location + 1.
            CONSTANTS
WRITE       DATA        X'01'         Write order.
READ        DATA        X'02'         Read order.
ORDER       DATA        0             Specified order.
            DATA        IOBUFFER      Starting address of I/O buffer area.
            DATA        0             Byte count + interrupt bit are stored here.
RADRETN     DATA        0             Return address to main program.
RADADDRS    DATA        X'F0'         Unit address of RAD.
ECHANNEL    DATA        X'16'         Even channel address.
OCHANNEL    DATA        X'17'         Odd channel address.
COUNT       DATA        0             Byte count.
ERRSAVE     DATA        0             Temporary storage for error bits.
INTCNTL     DATA        X'1200'       Arm and enable selected interrupts.
INTCNTLI    DATA        X'1100'       Disarm selected interrupts.
NOERXIT     DATA        WAIT          Interrupt WAIT.
ERREXIT     DATA        EXIT
            DATA        EXIT - 2
AIOSTAT     RES         2             AIO status storage registers.
TIOSTAT     RES         2             TIO status storage registers.
SEEK        DATA        X'03'         Seek order.
TRAKSECT    DATA        0             Track and sector address for specified operation.
            MAIN PROGRAM
              .
              .
              .
            RCPYI       1,2
            B           RADWRITE      Calling instruction for write operation.
            B           WDONE         Normal return.
            B           WABNORM       Abnormal return.
            B           WERROR        Error return.
              .
              .
              .
            RCPYI       1,2
            B           RADREAD       Calling instruction for read operation.
            B           RDONE         Normal return.
            B           RABNORM       Abnormal return.
            B           RERROR        Error return.
```